

IN THE CLAIMS:

- 1 1. (Cancelled) A method of forming a FinFET, comprising the steps
- 2 of:
- 3 forming a set of at least one semiconducting fin on a substrate;
- 4 forming a gate insulator on said set of fins;
- 5 depositing a layer of gate material over said set of fins;
- 6 forming a hardmask on said gate material extending perpendicular to said
- 7 set of fins and having a hardmask thickness;
- 8 etching said gate material outside said hardmask down to said substrate,
- 9 thereby forming a gate intersecting said set of fins and defining a body
- 10 region in said fins below said gate;
- 11 depositing a conformal layer of insulator enclosing said gate;
- 12 performing an anisotropic etch of said conformal layer, thereby exposing
- 13 said set of fins while said gate remains covered by said conformal layer of
- 14 insulator; and
- 15 forming source and drain regions in said fins, separated from said gate by
- 16 said conformal layer of insulator.

1 2. (cancelled) A method according to claim 1, further comprising the
2 steps of:
3 depositing a source/drain material over a set of at least two fins after said
4 anisotropic etch of said conformal layer, thereby making contact with sides
5 of said at least two fins and forming a FinFET having at least two fins.

1 3. (cancelled) A method according to claim 2, further comprising a
2 step of:
3 recessing said source/drain material to substantially the height of said set
4 of fins; and
5 forming source/drain contacts on a top surface of said source/drain
6 material.

1 4. (cancelled) A method according to claim 2, in which said fins and
2 said gate are formed from silicon and further comprising the steps of:
3 exposing silicon in said fins and in an upper portion of said gate; and
4 performing a silicidation step of said exposed silicon.

1 5. (currently amended) A method ~~according to claim 2~~ of forming a
2 FinFET, further comprising the steps of:

3 forming a set of at least one semiconducting fin on a substrate;

4 forming a gate insulator on said set of fins;

5 depositing a layer of gate material over said set of fins;

6 forming a hardmask on said gate material extending perpendicular to said

7 set of fins and having a hardmask thickness;

8 etching said gate material outside said hardmask down to said substrate,

9 thereby forming a gate intersecting said set of fins and defining a body

10 region in said fins below said gate;

11 depositing a conformal layer of insulator enclosing said gate;

12 performing an anisotropic etch of said conformal layer, thereby exposing

13 said set of fins while said gate remains covered by said conformal layer of

14 insulator by depositing a source/drain material over a set of at least two

15 fins after said anisotropic etch of said conformal layer, thereby making

16 contact with sides of said at least two fins and forming a FinFET having at
17 least two fins;
18 forming source and drain regions in said fins, separated from said gate by
19 said conformal layer of insulator; and
20 depositing a blocking material over a set of FinFET locations and opening
21 an aperture over a subset of locations for a first polarity of FinFETs;
22 depositing a second conformal insulating layer over gates in said locations
23 for a first polarity of FinFETs, said second layer having a separation
24 thickness combined with said first layer such that dopant material in
25 sources and drains of said first polarity of FinFETs are separated from said
26 gates.

1 6. (original) A method according to claim 2, in which:
2 said hardmask thickness is such that a remaining layer of said hardmask
3 remains above said gate after said anisotropic etch when said fins are
4 exposed by removing said conformal layer of insulator down to said
5 substrate.

1 7. (original) A method according to claim 1, in which said fins and
2 said gate are formed from silicon and further comprising the steps of:
3 exposing silicon in said fins and in an upper portion of said gate; and
4 performing a silicidation step of said exposed silicon.

1 8. (currently amended) A method ~~according to claim 1~~ of forming a
2 FinFET, further comprising the steps of:
3 forming a set of at least one semiconducting fin on a substrate;
4 forming a gate insulator on said set of fins;
5 depositing a layer of gate material over said set of fins;
6 forming a hardmask on said gate material extending perpendicular to said
7 set of fins and having a hardmask thickness;
8 etching said gate material outside said hardmask down to said substrate,
9 thereby forming a gate intersecting said set of fins and defining a body
10 region in said fins below said gate;
11 depositing a conformal layer of insulator enclosing said gate;
12 performing an anisotropic etch of said conformal layer, thereby exposing
13 said set of fins while said gate remains covered by said conformal layer of
14 insulator; and

15 forming source and drain regions in said fins, separated from said gate by
16 said conformal layer of insulator by depositing a source/drain material over
17 a set of at least two fins after said anisotropic etch of said conformal layer,
18 thereby making contact with sides of said at least two fins and forming a
19 FinFET having at least two fins;
20 further comprising a step of depositing a blocking material over FinFET
21 locations and opening an aperture over locations for a first polarity of
22 FinFETs;
23 depositing a second conformal insulating layer over gates in said locations
24 for a first polarity of FinFETs, said second layer having a separation
25 thickness combined with said first layer such that dopant material in
26 sources and drains of said first polarity of FinFETs are separated from said
27 gates.

1 9. (original) A method according to claim 8, further comprising the
2 steps of:
3 depositing a source/drain material over a set of at least two fins after said
4 anisotropic etch of said conformal layer, thereby making contact with sides
5 of said at least two fins and forming a FinFET having at least two fins.

1 10. (original) A method according to claim 9, in which;
2 said hardmask thickness is such that a remaining layer of said hardmask
3 remains above said gate after said anisotropic etch when said fins are
4 exposed by removing said conformal insulating layer down to said
5 substrate.

1 11. (original) A method according to claim 9, in which said fins, said
2 S/D material and said gate are formed from silicon and further comprising
3 the steps of:
4 exposing silicon in said fins and S/D material and in an upper portion of
5 said gate; and
6 performing a silicidation step of said exposed silicon.

1 12. (original) A method according to claim 11, further comprising a
2 step of:
3 after said step of silicidation, removing said conformal layer over said
4 gate, thereby forming an aperture between said gate and said S/D material
5 having a vertical exposed silicon gate surface; and

6 performing a step of silicidation on said exposed gate surface.

1 13. (cancelled) A method according to claim 1, in which;
2 said hardmask thickness is such that a remaining layer of said hardmask
3 remains above said gate after said anisotropic etch when said fins are
4 exposed by removing said conformal insulating layer down to said
5 substrate.

1 14. (cancelled) A method according to claim 13, in which;
2 said hardmask thickness is such that a remaining layer of said hardmask
3 remains above said gate after said anisotropic etch when said fins are
4 exposed by removing said conformal insulating layer down to said
5 substrate.

1 15. (currently amended) A method ~~according to claim 13~~ of forming a
2 FinFET, comprising the steps of:
3 forming a set of at least one semiconducting fin on a substrate;
4 forming a gate insulator on said set of fins;
5 depositing a layer of gate material over said set of fins;

6 forming a hardmask on said gate material extending perpendicular to said
7 set of fins and having a hardmask thickness;
8 etching said gate material outside said hardmask down to said substrate,
9 thereby forming a gate intersecting said set of fins and defining a body
10 region in said fins below said gate;
11 depositing a conformal layer of insulator enclosing said gate;
12 performing an anisotropic etch of said conformal layer, thereby exposing
13 said set of fins while said gate remains covered by said conformal layer of
14 insulator; and
15 forming source and drain regions in said fins, separated from said gate by
16 said conformal layer of insulator, in which said fins, said S/D material and
17 said gate are formed from silicon;
18 said hardmask thickness is such that a remaining layer of said hardmask
19 remains above said gate after said anisotropic etch when said fins are
20 exposed by removing said conformal insulating layer down to said
21 substrate;
22 and further comprising the steps of:
23 exposing silicon in said fins and S/D material and in an upper portion of
24 said gate; and

25 performing a silicidation step of said exposed silicon.

1 16. (original) A method according to claim 15, further comprising a
2 step of:
3 after said step of silicidation, removing said conformal layer over said
4 gate, thereby forming an aperture between said gate and said S/D material
5 having a vertical exposed silicon gate surface; and
6 performing a step of silicidation on said exposed gate surface.

1 17. (currently amended) A method ~~according to claim 2~~ of forming a
2 FinFET,
3 comprising the steps of:
4 forming a set of at least one semiconducting fin on a substrate;
5 forming a gate insulator on said set of fins;
6 depositing a layer of gate material over said set of fins;
7 forming a hardmask on said gate material extending perpendicular to said
8 set of fins and having a hardmask thickness;

9 etching said gate material outside said hardmask down to said substrate,
10 thereby forming a gate intersecting said set of fins and defining a body
11 region in said fins below said gate;
12 depositing a conformal layer of insulator enclosing said gate;
13 performing an anisotropic etch of said conformal layer, thereby exposing
14 said set of fins while said gate remains covered by said conformal layer of
15 insulator; and
16 forming source and drain regions in said fins, separated from said gate by
17 said conformal layer of insulator by depositing a source/drain material over
18 a set of at least two fins after said anisotropic etch of said conformal layer,
19 thereby making contact with sides of said at least two fins and forming a
20 FinFET having at least two fins , in which said fins, said S/D material and
21 said gate are formed from silicon and further comprising the steps of:
22 exposing silicon in said fins and S/D material and in an upper portion of
23 said gate; and
24 performing a silicidation step of said exposed silicon.

1 18. (original) A method according to claim 17, further comprising a
2 step of:

3 after said step of silicidation, removing said conformal layer over said
4 gate, thereby forming an aperture between said gate and said S/D material
5 having a vertical exposed silicon gate surface; and
6 performing a step of silicidation on said exposed gate surface.

1 19. (cancelled) An integrated circuit comprising at least one FinFET
2 comprising:
3 a set of at least one semiconducting fin(s) on a substrate;
4 said set of fins having a gate insulator separating a body region thereof
5 from a selfaligned gate formed by etching a layer of gate material disposed
6 over said set of fins outside a hardmask down to said substrate, thereby
7 forming a gate intersecting said set of fins and defining said body region in
8 said fins below said gate;
9 a separation layer of insulator enclosing said gate and formed by an
10 anisotropic etch of a conformal layer, that exposed said set of fins while
11 said gate remained covered by said conformal layer of insulator; and
12 source and drain regions in said fins, selfaligned to said gate and separated
13 from said gate by said conformal layer of insulator.

1 20. (cancelled) An integrated circuit according to claim 19, in which
2 said set of fins comprises at least two fins having a source portion and a
3 drain portion, at least one of which source and drain portions are in
4 electrical contact with a S/D material on vertical sides thereof.

1 21. (cancelled) An integrated circuit according to claim 20, in which
2 said S/D material is recessed below a top of said gate and above a top of
3 said fins.

1 22. (cancelled) An integrated circuit according to claim 21, in which
2 said S/D material is silicon and a portion thereof is silicide.

1 23. (currently amended) An integrated circuit ~~according to claim 19~~
2 comprising at least one FinFET comprising:
3 a set of at least one semiconducting fin(s) on a substrate;
4 said set of fins having a gate insulator separating a body region thereof
5 from a selfaligned gate formed by etching a layer of gate material disposed
6 over said set of fins outside a hardmask down to said substrate, thereby

7 forming a gate intersecting said set of fins and defining said body region in
8 said fins below said gate;
9 a separation layer of insulator enclosing said gate and formed by an
10 anisotropic etch of a conformal layer, that exposed said set of fins while
11 said gate remained covered by said separation layer of insulator; and
12 source and drain regions in said fins, selfaligned to said gate and separated
13 from said gate by said separation layer of insulator, in which a first subset
14 of N-type FinFETs has a first thickness of said separation layer and a
15 second subset of P-type FinFETs has a second thickness of separation
16 layer, said second thickness being greater than said first thickness.